CLAIMS

Having thus described our invention in detail, what we claim as new is:

1. A method of fabricating an integrated semiconductor structure comprising:

providing a structure comprising a carrier wafer and at least a film stack of a first semiconductor layer of a first crystallographic orientation and an overlying second semiconductor layer of a second crystallographic orientation, said first crystallographic orientation is different from said second crystallographic orientation;

forming at least one opening in the structure that exposes a surface of the first semiconductor layer;

forming a semiconductor material in the at least one opening on the exposed surface of the first semiconductor layer, said semiconductor material having the same crystallographic orientation as the first semiconductor layer;

forming an insulator layer on the structure and bonding the insulator to a handling wafer;

selectively removing the carrier wafer and first semiconductor layer to expose a surface portion of the semiconductor material; and

etching back the surface portion of the semiconductor material to provide a structure in which the etched back semiconductor material having the first crystallographic orientation is substantially coplanar and of substantially the same thickness as that of the second semiconductor layer.

2. The method of Claim 1 wherein an optional etch stop layer is formed between the carrier wafer and the first semiconductor layer.

3. The method of Claim 1 wherein the carrier wafer and the first semiconductor wafer are components of a silicon-on-insulator substrate that is formed by a separation by ion implantation of oxygen process.

4. The method of Claim 1 further comprising forming an insulator between the first semiconductor layer and the second semiconductor layer.

5. The method of Claim 1 wherein the structure is provided by bonding the second semiconductor layer to the first semiconductor layer.

6. The method of Claim 5 wherein said bonding comprising a heating step that is performed in an inert ambient at a temperature of from about 200°C to about 1300°C.

7. The method of Claim 1 wherein said at least one opening is formed by providing a patterned masking layer above the second semiconductor layer by deposition and lithography, and etching.

8. The method of Claim 7 further comprising a pad layer formed prior to formation of the patterned masking layer.

9. The method of Claim 1 wherein said at least one opening further comprises spacers located on sidewalls thereof.

10. The method of Claim 1 wherein said semiconductor material is formed by an epitiaxial growth process.

11. The method of Claim 1 wherein said etch back comprises a reactive ion etching process.

12. The method of Claim 1 further comprising forming at least one pFET and a least one nFET on said structure.

13. The method of Claim 12 wherein the at least one pFET is located on a (110) crystallographic surface, while the at least one nFET is located on a (100) crystallographic surface.

14. The method of Claim 1 wherein the second semiconductor layer has a (110) surface orientation and the semiconductor material has a (100) surface orientation.

15. The method of Claim 14 further comprising forming at least one pFET on the (110) surface and at least one nFET the (100) surface.

16. A method of fabricating a strained-silicon-direct-on-insulator comprising:

providing a structure comprising a carrier wafer, at least a film stack of a first semiconductor layer of a first crystallographic orientation and an overlying second semiconductor layer of a second crystallographic orientation, said first crystallographic orientation is different from said second crystallographic orientation, a first graded SiGe alloy layer atop the second semiconductor layer and a first strained Si layer atop the first graded SiGe alloy layer;

forming at least one opening in the structure that exposes a surface of the first semiconductor layer;

forming a second graded SiGe alloy layer and an overlying second strained Si layer in the at least one opening on the exposed surface of the first semiconductor layer, said first and second strained Si layers having different crystallographic orientations;

forming an insulator layer on the structure and bonding the insulator to a handling wafer;
selectively removing the carrier wafer, first semiconductor layer and the second semiconductor layer to expose the second graded SiGe alloy; and

removing the second graded SiGe alloy layer and the first graded SiGe alloy to provide a structure in which first stained Si layer is substantially coplanar and of substantially the same thickness as that of the second strained Si layer.

17. A method of fabricating a strained-silicon-direct-on-insulator comprising:

providing a planar structure comprising a carrier wafer, at least a film stack of a first semiconductor layer of a first crystallographic orientation and an overlying second semiconductor layer of a second crystallographic orientation, said first crystallographic orientation is different from said second crystallographic orientation, and an opening the extends to the first semiconductor layer, said opening containing a second graded SiGe alloy layer, a second strained Si layer, and a masking cap;

forming a first graded SiGe alloy layer and an overlying first strained Si layer atop the second semiconductor material abutting the at least one opening, said first and second strained Si layer having different crystallographic orientations;

forming an insulator layer on the structure and bonding the insulator to a handling wafer;

selectively removing the carrier wafer, first and second semiconductor layers, and the first and second graded SiGe alloys to provide a structure in which first stained Si layer is substantially coplanar and of substantially the same thickness as that of the second strained Si layer.

18. A strained-silicon-direct-on-insulator (SSDOI) comprising at least an SOI substrate comprising a first strained Si of a first crystallographic orientation and a second strained Si layer of a second crystallographic orientation, wherein the second strained Si layer is substantially coplanar and of substantially the same thickness as that of the first strained Si layer and said first crystallographic orientation is different from the second crystallographic orientation.

19. The SSDOI of Claim 18 wherein the first strained Si has a (110) surface orientation and the second strained Si layer has a (100) surface orientation.

20. The integrated semiconductor structure of Claim 19 further comprising at least one pFET located on the (110) surface orientation and at least one nFET located on the (100) surface orientation.

21. The integrated semiconductor structure of Claim 18 wherein the first strained Si layer has a (100) surface orientation and the second strained Si layer has a (110) surface orientation.

22. The integrated semiconductor structure of Claim 21 further comprising at least one pFET located on the (110) surface orientation and at least one nFET located on the (100) surface orientation.

23. The integrated semiconductor structure of Claim 18 further comprising at least one pFET and at least one nFET, each device is located on either the first strained Si layer or the second strained Si layer, said location being dependent on the crystallographic orientation.

24. The integrated semiconductor structure of Claim 23 wherein the at least one pFET is located on a (110) or a (111) crystal orientation, while the at least one nFET is located on a (100) or a (111) crystal orientation.